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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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ARMSTRONG, KRATZ, QUINTOS, HANSON & BROOKS, LLP
1725 K STREET, NW
SUITE 1000
WASHINGTON, DC 20006

EXAMINER	
FULK, STEVEN J	

ART UNIT	PAPER NUMBER
2891	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/532,249	MARUYAMA ET AL.	
	Examiner	Art Unit	
	Steven J. Fulk	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-23* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/22/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *Foreign reference*.

DETAILED ACTION

Claim Objections

1. Claims 1-3 are objected to because of the following informalities: Claims 1-3 recite the limitation "the other circuit of the semiconductor device". There is insufficient antecedent basis for the limitation "the other circuit of the semiconductor device" in the claims. Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 4, 5 and 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeshi et al. (Abstract JP8186235) in view of Mirkarimi et al. '094.

a. Regarding claims 1, 4, 5 and 9, Takeshi et al. discloses a method of producing a semiconductor device incorporating a capacitor structure that includes a ferroelectric thin film, comprising: forming, on a single crystalline substrate (figure A, memory capacitor part 10) having a surface suited for growing thereon a thin film layer of ferroelectric single crystal having a plane (111), an electrically conducting thin film that will form one electrode of the capacitor on the single crystalline substrate; forming a ferroelectric single

crystalline thin film containing Pb or a ferroelectric polycrystalline thin film containing Pb ($PbZrTiO_3$ layer 6, which would inherently be either single crystalline or polycrystalline); wherein the single crystalline substrate has a plane (111) on which the ferroelectric thin film is to be formed, or a single crystalline substrate having an offset angle from the plane (111) is used (the substrate would inherently have either a (111) plane or another plane that is offset from the (111) plane); and part of a circuit of a semiconductor device (metal bumps 1), to thereby fabricate a single crystalline substrate having the ferroelectric thin film containing Pb and the part of the circuit of the semiconductor device; and bonding the single crystalline substrate to another substrate (transistor part 20) on which the other circuit of the semiconductor device has been formed in advance, to couple the two circuits together to thereby obtain a semiconductor device incorporating a capacitor structure that includes a ferroelectric thin film (figure B).

Takeshi et al. does not explicitly disclose the ferroelectric thin film to have a plane (111) in parallel with the surface of the substrate. Mirkarimi et al. teaches a ferroelectric memory device wherein the ferroelectric thin film has a (111) orientation. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the (111) oriented thin film of Mirkarimi et al. as the thin film of Takeshi et al. One would have been motivated to do this because Mirkarimi et al. taught that the (111) orientation of PZT minimized the electromechanical coefficient of the material, thus minimizing physical distortion of the layer and preventing

damage to the memory device (Mirkarimi et al., col. 1, lines 14-35 and col. 2, lines 20-28).

b. Regarding claim 10, Takeshi et al. discloses all of the elements of the claims as set forth in paragraph 3a above, but the reference does not explicitly disclose the electrically conducting thin film to be formed of Pt, Ir, Ti, Ru or an oxide thereof. Mirkarimi et al. teaches the use of Pt or Ir as the electrically conducting thin film.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the Pt or Ir electrode material of Mirkarimi et al. in the method of Takeshi et al. One would have been motivated to do this because Mirkarimi et al. taught that Pt and Ir were conventionally electrode materials used with ferroelectric capacitors due to their lattice constants being similar to the ferroelectric materials (Mirkarimi et al., col. 3, line 64 – col. 4, line 1), thus reducing strain between the layers and improving the performance of the device.

c. Regarding claims 11 and 12, Takeshi et al. discloses all of the elements of the claims as set forth in paragraph 3a above, but the reference does not explicitly disclose the substrate to comprise single crystalline silicon having a plane {111}, {100} or offset from {111} or {100}. Mirkarimi et al. teaches the use of a silicon substrate, which would inherently have a plane {111}, {100} or offset from {111} or {100}.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the substrate of Mirkarimi et al. in the

method of Takeshi et al. because single crystalline silicon was a well known, conventional substrate used in semiconductor manufacturing due to its process compatibility and low cost.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takeshi et al. (Abstract JP8186235) in view of Mirkarimi et al. '094, and further in view of Adkisson et al. '202.

Takeshi et al. in view of Mirkarimi et al. teach all the elements of the claim as set forth above, and Takeshi et al. also discloses patterning the thin film layer to thereby form isolated ferroelectric thin films of a predetermined shape on the single crystalline substrate, forming one electrode of a capacitor of a predetermined shape positioned on the ferroelectric thin film, but the references do not explicitly disclose removing the single crystalline substrate to expose the ferroelectric thin film, and forming another electrode of the capacitor on the ferroelectric thin film that is exposed.

Adkisson et al. teaches a method of forming a ferroelectric capacitor device wherein a ferroelectric thin film (fig. 1b, 30) is formed on a single crystalline substrate (24), the single crystalline substrate is bonded to another substrate having a circuit formed in advance (fig. 1a, 10; fig. 1c), and the single crystalline substrate is removed (fig. 1d). It would have been obvious to one of ordinary skill in the art at the time the invention was made to remove the single crystalline substrate in the method of Takeshi et al. in view of Mirkarimi et al. as taught by Adkisson et al. One would have been motivated to do this because removing the single crystalline substrate allowed the top of the ferroelectric device to be

contacted by an electrode and connected to peripheral circuitry, thus allowing the device to perform its intended function.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takeshi et al. (Abstract JP8186235) in view of Mirkarimi et al. '094, and further in view of Kim et al. '371.

Takeshi et al. in view of Mirkarimi et al. teach all the elements of the claim as set forth above, but the references do not explicitly disclose the substrate to be MgO or $SrTiO_3$. Kim et al. discloses a ferroelectric capacitor device wherein the substrate is MgO (fig. 1a, 11). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the MgO substrate of Kim et al. in the method as taught by Takeshi et al. in view of Mirkarimi et al. One would have been motivated to do this because MgO was a conventional substrate used with PZT material due to its similar lattice constant.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takeshi et al. (Abstract JP8186235) in view of Mirkarimi et al. '094, and further in view of Greenwald et al. '026.

Takeshi et al. in view of Mirkarimi et al. teaches all the elements of the claim as set forth above, but the references do not explicitly disclose the substrate to be an a-Al_2O_3 single crystalline substrate having a plane (0001) on which the ferroelectric thin film is to be formed, or an a-Al_2O_3 single crystalline substrate having an offset angle from the plane (0001). Greenwald et al. discloses a ferroelectric capacitor device wherein the substrate is a-Al_2O_3 (fig. 1, 10), which would inherently have a plane (0001) or a plane offset from (0001). It would have

been obvious to one of ordinary skill in the art at the time the invention was made to use the a-Al_2O_3 substrate of Greenwald et al. in the method as taught by Takeshi et al. in view of Mirkarimi et al. One would have been motivated to do this because a-Al_2O_3 was a conventional substrate used with PZT material due to its similar lattice constant.

7. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takeshi et al. (Abstract JP8186235) in view of Mirkarimi et al. '094, and further in view of Yamawaki et al. '774.

Takeshi et al. in view of Mirkarimi et al. teaches all the elements of the claim as set forth above, but the references do not explicitly disclose the substrate to be $MgAl_2O_4$. Yamawaki et al. discloses a ferroelectric capacitor device wherein the substrate is $MgAl_2O_4$ (fig. 4, 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the $MgAl_2O_4$ substrate of Yamawaki et al. in the method as taught by Takeshi et al. in view of Mirkarimi et al. One would have been motivated to do this because $MgAl_2O_4$ was a conventional substrate used with PZT material due to its similar lattice constant.

8. Claims 13-18 and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeshi et al. (Abstract JP8186235) in view of Mirkarimi et al. '094, and further in view of Li '254.

Takeshi et al. in view of Mirkarimi et al. teaches all the elements of the claim as set forth above, including an electrically conducting film that is a stack of Pt or Ir before forming the ferroelectric thin film, but the references do not explicitly disclose the epitaxially forming the ferroelectric thin film through a buffer layer of

MgO. Li teaches a method of epitaxially forming a ferroelectric thin film through a buffer layer of MgO. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the MgO buffer layer of Li in the method as taught by Takeshi et al. in view of Mirkarimi et al. One would have been motivated to do this because Li taught that a buffer layer provided excellent crystalline properties and surface flatness of the ferroelectric thin film (Li, ¶[0024]), thus improving the performance of the device.

9. Claims 19 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeshi et al. (Abstract JP8186235) in view of Mirkarimi et al. '094, further in view of Li '254, and further in view of Lee et al. '705.

Takeshi et al. in view of Mirkarimi et al., and further in view of Li teaches all the elements of the claim as set forth above, including an electrically conducting thin film, but the references do not explicitly disclose the electrically conducting thin film to be formed of $SrRuO_3$, YBCO or LSCO. Lee et al. teaches a method of forming a ferroelectric thin film capacitor wherein the electrically conducting thin film is formed of $SrRuO_3$ or LSCO (col. 4, lines 36-40). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the $SrRuO_3$ or LSCO conducting film of Lee et al. in the method as taught by Takeshi et al. in view of Mirkarimi et al., and further in view of Li. One would have been motivated to do this because Lee taught that $SrRuO_3$ or LSCO were art recognized functional equivalents of Pt and Ir (Lee et al., col. 4, lines 36-40) (MPEP § 2144.06).

Allowable Subject Matter

9. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter: a search of the prior art failed to disclose or reasonably suggest a method of producing a ferroelectric thin film capacitor comprising forming an electrically conducting thin film layer on a single crystalline substrate having through holes, forming, on said electrically conducting thin film layer, ferroelectric thin film containing Pb and having a plane (111) in parallel with the surface of the substrate, patterning said electrically conducting thin film layer and said ferroelectric thin film layer to thereby form isolated ferroelectric thin films of a predetermined shape and one electrode of a capacitor of a predetermined shape, forming another electrode of the capacitor on said ferroelectric thin film, and forming part of a circuit of a semiconductor device so as to pass through the holes in said single crystalline substrate, to thereby fabricate a single crystalline substrate comprising a capacitor structure constituted by said ferroelectric thin film containing Pb and a pair of electrodes holding the ferroelectric thin film there between, as recited by claim 3.

Takeshi et al. (JP8186235), Mirkarimi et al. '094, Adkisson et al. '202, Kim et al. '371, Greenwald et al. '026, Yamawaki et al. '774, Li '254 and Lee et al. '705 disclose a method of forming a ferroelectric thin film capacitor, but the references do not teach the limitations of claim 3 as discussed above.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven J. Fulk whose telephone number is (571) 272-8323. The examiner can normally be reached on Monday through Friday, 9:30am to 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SJF

Steven J. Fulk
Patent Examiner
Art Unit 2891

June 21, 2007

B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINER